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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,763	08/30/2001	Shuba Swaminathan	M4065.0459/P459	7372

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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,763	SWAMINATHAN, SHUBA	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-96* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14,31,32,37,45,58,65,66,71,84,89,90 and 96* is/are allowed.

6)☒ Claim(s) *1-13,15-30,33-36,38-44,46-57,59-64,67-70,72-83,85,88 and 91-95* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 3 and 26 are objected to because of the following informalities:

The limitation "memory block to be erased" should be changed to "erase block" or "erase memory block". The portion of the specification that supports this claim is paragraph 33 on page 7. The specification uses the term "erase block" which is a unit of memory in a flash array that is erased together at one time. The term of art "erase block" does not mean a "memory block to be erased". Although this limitation may not be technically incorrect, since all flash memory blocks are erased before being written to, "memory block to be erased" is a mistranslation of a term of art, which simply designates a unit of memory.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 8, 9, 22, 23, 52, 53, 77 and 78 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a refresh operation of multiple erase blocks to be performed one erase block at a time after a processor initiated operation per erase block, does not reasonably provide enablement for dividing data/region into pieces during the refreshing step. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with

these claims. The specification discloses that when multiple erase blocks need to be refreshed, each erase block that requires refreshing is refreshed after an operation initiated by the processor. This does not support the claimed limitation that requires dividing the data in the block to be erased (claim 22, for example) into pieces in the refreshing step.

4. Claims 50 and 76 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for refreshing an erase block in the same location, does not reasonably provide enablement for restoring/refreshing data into the erased memory block. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. The main concept disclosed in the specification is to refresh erase blocks that are affected by disturb effects caused by erasures of nearby erase blocks. The specification does not describe a situation where the data to be erased is restored in the erased erase block during the refresh step of the claimed methods. Examiner further notes that although the claims do not exclude the possibility, one skilled in the art can easily discern, from the disclosure, that the erased block is not one of the blocks that are refreshed, since when a block is erased its counter is reset to zero making it unlikely to exceed the preset threshold.

For the purposes of this examination "said erased memory block" will be interpreted as "said memory block" or "said memory region".

5. Claims 15, 38, 59, 72, 82 and 94 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which

was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claims require that each bit of an entry correspond to one memory block of N based on the bit's position within the entry. Figure 4 and paragraph 30 on page 6 of the specification clearly show that the first two bytes of an entry are fixed values that are used as delimiters and are unrelated to N memory blocks. While the specification discloses that some bits correspond to one memory block of N, it also discloses that some bits clearly do not correspond to one of N memory blocks. The examiner also notes that the claims do not require that each entry contain N data bytes.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 21, 22, 23, 27, 75, 76 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claims 21 and 22 recite the limitation "said data" in line 1, respectively. There is insufficient antecedent basis for this limitation in the claims. Claim 23 depends from claim 22.

9. Claim 27 improperly depends from itself. It is not clear what the scope of the claim is.

10. Claims 75 and 76 recite the limitations "said memory blocks" and "said erased memory block", respectively. There are insufficient antecedent bases for these limitations in the claims.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1 – 7, 10 – 12, 17 – 21, 47 – 51, 54 – 56, 73 – 75 and 79 – 81 are rejected under 35 U.S.C. 102(b) as being anticipated by Norman (US Patent No. 5,715,193).

13. With respect to claims, 1, 17, 47 and 73, Norman discloses a processor circuit (figure 3) comprising:

a processor (129, col. 10, lines 43 – 46); and

a flash memory storage device (16) coupled to said processor, said flash memory storage device comprising a plurality of memory storage regions (16E) and a plurality of counters, each of said plurality of counters associated with one of said plurality of memory storage regions;

wherein when data stored in one of said memory storage regions is erased, the counter associated with said memory storage region is set to a first predetermined value and the remaining counters are incremented (col. 11, lines 14 – 16); and

wherein when one of said plurality of counters equals or exceeds a predetermined threshold value, the data in the memory storage region associated with said counter is refreshed (col. 11, lines 36 – 38).

14. With respect to claims 10 – 12, 54 – 56 and 79 – 81, the values of said counters are stored in a table (col. 11, lines 12 – 13) in the flash memory array (16) and in a separate memory storage device (25).

15. With respect to claims 2, 19 and 74, said first predetermined value is zero (col. 11, 26 – 27, see also the table update example in col. 12).

16. With respect to claims 3, 4, 20, 48 and 75, wherein said refreshing comprises storing data from a memory block to be erased in a different block in said flash memory array or in a different flash memory array (col. 13, lines 52 – 55).

17. With respect to claims 5, 6, 21, 49, 50 and 76, said refreshing comprises restoring said data from said memory block in said memory block in the same locations in a memory block as it is read from (figures 4A, 4B, steps 212, 218238, and 241, see also col. 13, lines 28 – 59).

18. With respect to claims 7 and 51, refreshing further comprises optimizing the locations said data is stored in (col. 13, lines 28 – 59, the refreshing step optimizes the location for the data by moving data from sectors that are "old" or "obsolete" when a rewrite fails).

19. With respect to claim 16, entries in said table contain eight data bytes (figure 2, the figure shows at least 64 erase blocks which translates to at least 64 entries). Examiner notes that the

claim does not require that each entry contain eight bytes. It merely requires that the table contain eight bytes of entry data.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 24 – 30, 33 – 35, 39 – 45, 60 – 64, 67 - 69, 85 – 88 and 91 – 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Norman.

22. With respect to claims 24, 40, 60, and 85, Norman discloses a processor circuit (figure 3) comprising:

a processor (129, col. 10, lines 43 – 46); and

a flash memory storage device (16) coupled to said processor, said flash memory storage device comprising a plurality of memory storage regions (16E, decode block), said memory storage regions being divided into a plurality of sectors (figure 2, 16B erase blocks), and a plurality of counters (col. 11, lines 5 – 13) , each of said plurality of counters associated with one of said sectors;

wherein when an operation on one of said sectors causes a disturb effect (col. 8, lines 42 – 55,), the counter associated with said sector is set to a first predetermined value and all of the sectors adjacent to said programmed sector incremented (col. 11, lines 14 – 16); and

wherein when one of said plurality of counters equals or exceeds a predetermined threshold value, the data in the sector associated with said counter is refreshed (col. 11, lines 36 – 38).

However, Norman does not specifically disclose that an operation that causes a disturb effect, that triggers the counters to be incremented, is a sector programming operation. On the other hand, Norman discloses that each time a block is erase or programmed, a disturb effect affects other blocks (col. 1, lines 27 – 30), clearly recognizing that both programming and erasing cause disturb effects. Norman also discloses that "maximum value" of the disturb count for an erase block, for triggering a refresh operation, is determined from some combination of the program disturb and erasure disturb times (col. 11 line 66 – col. 12, line 6). Norman further shows a concrete example of how to calculate a maximum value of the disturb count for erasures when the weight give to the programming disturb time is zero.

It would have been obvious to one of ordinary skill in the art, having the teachings of Norman before him at the time the invention was made, to recognize that when the program disturb time is given weight other than zero the system would need to keep track of programming disturb events as claimed since the maximum value of the disturb count would now include disturb count due to programming. Keeping track of disturb effect due to programming as well as erasing allows one to keep more accurate count of the overall disturb effects and not just effects due to one type of operation.

23. With respect to claims 33 – 35, 67 – 69 and 91 – 93, see rejections of claims 10 – 12 above.

24. With respect to claims 25, 42 and 86, see rejection of claim 2 above.

25. With respect to claims 26, 43, 61 and 87, see rejections of claims 3 – 4 above.

26. With respect to claims 28, 29, 44, 62, 63 and 88, see rejections of claims 5 – 6 above.

27. With respect to claims 30 and 64, see rejection of claim 7 above.

28. With respect to claim 39, see rejection of claim 16 above.

29. Claims 18 – 21 and 41 – 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Norman in view of Kon (US Patent No. 6,249,838).

30. With respect to claims 18 and 41, Norman discloses all of the limitations of claims 17 and 40 as discussed above. The only difference between the two sets of claims is the method of determining the number of disturbance events, i.e. erasures and writes. Claims 18 and 41 decrement the counters while claims 17 and 40 increment the counters to keep track of the number of events that causes disturbance for the purpose of determining whether refresh

operation are needed. There is no patentable difference between the two methods of keeping track of the event counts since they are equivalent operations performed to obtain the same results (keep total count of events) for the same purpose (to determine whether a block needs to be refreshed). In addition, Kon explicitly discloses a method of keeping track of events by decrementing a counter for each disturbance event, i.e. erase, until a threshold is reached for appropriate actions (abstract).

It would have been obvious to one of ordinary skill in the art, having the teachings of Kon and Norman before him at the time the invention was made, to use the decrementing the counter to reach a threshold teachings of the flash memory of Kon in the flash memory of Norman, in order to keep track of the total number of erasures to determine the remaining life expectancy.

31. With respect to claims 19 – 21 and 42 – 44, see rejections of claims 2 – 6 above.

32. Claims 13, 36, 57, 70, 83 and 95 are rejected under 35 U.S.C. 103(a) as being unpatentable over Norman in view of Bruce *et al.* (US Patent No. 6,000,006, hereinafter "Bruce").

Norman either discloses all of the limitations of the parent claims or limitations that are not specifically disclosed by Norman are obvious as discussed above. However, Norman does not specifically disclose that the most significant byte and the second most significant byte of each entry in said table are set to predetermined binary values. On the other hand, Bruce

discloses a flash memory system that keeps track of erasure counts in a table (figure 5, write count is equivalent to an erasure count since every write must be preceded by an erasure in a memory) where the most significant byte and the second most significant byte of each entry are set to predetermined binary values (figure 5, 44, and col. 11, lines 27 – 47, the two most significant byte in the entry are the two most significant bytes of the 4 byte physical address, physical address of an entry is predetermined).

It would have been obvious to one of ordinary skill in the art, having the teachings of Bruce and Norman before him at the time the invention was made, to use the unified re-map and cache-index index table with erasure counters teachings of the flash memory system with disturbance count table of Bruce in the flash memory system with disturbance count table of Norman, in order to take advantage of numerous benefits of the unified table disclosed by Bruce (col. 12, line 12 – col. 13, line 18). For example, a single lookup for multiple functions (col. 12, lines 44 – 50), elimination of tag RAM to reduce the cost of cache (col. 12, lines 1 – 53), improved error correction capabilities (col. 12, line 61 – col. 13, line 2), and a capability to rebuild the re-map table (col. 13, lines 3 – 8) are some of the benefits of using Bruce's teachings.

Allowable Subject Matter

33. Claims 14, 31, 32, 37, 45, 46, 58, 65, 66, 71, 84, 89, 90 and 96 are allowed.

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Katayama et al. (US Patent No. 6,480,416), Fukutomo (US Patent No. 6,240,032),

Chevallier (US Patent No. 6,493,270), Shinohara (US Patent No. 5,724,285) and Chou et al. (US Patent No. 6,639,839) disclose other non-volatile EEPROM systems that refresh their storage cells.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (703) 305-3845. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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whc
June 10, 2004

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100